Appl. No. **Applicant** Filed

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David L. Collins January 8, 2004

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TC/A.U. Examiner

Dudek Jr., Edward J.

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Customer No.

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Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450

## **DECLARATION UNDER 37 C.F.R. § 1.131**

Confirmation No. 6597

Sir:

1. I, David L. Collins, do declare and state:

- 2. I am the sole inventor of claims 1-10, 12-20 and 23-25 of the aboveidentified application.
- 3. The flowchart attached hereto was prepared by me or under my direct supervision. All work and associated writings were carried out in the United States.
- 4. All dates on the attached exhibits have been masked unless otherwise stated herein by reference to specific dates.
- 5. Prior to October 16, 2003, I completed my invention as described and claimed in the above-identified application, as evidenced by the following:

According to the procedure shown in the attached flowchart, I prepared a test program that upon reset of a computer (i.e. starting computer memory initialization) 1). determined whether the reset was firmware initiated. If the reset was NOT firmware initiated, then 2). stackless memory initialization code was executed to initialize a first memory controller and a portion of memory associated with this controller, 3). a software stack and variables were then initialized, 4). using the stack and variables, full stack-based memory initialization code was executed for the first memory controller to use the full memory associated with this controller, 5). formatted memory controller configuration data was thus generated for the first memory controller

and its associated memory, and the data was saved in an EEPROM of a memory module, and 6). a "firmware reset" flag was then set and a "reset" was executed. Following the reset of the computer after performance of the above portion of this procedure (i.e. upon restarting the computer memory initialization), this procedure then 7). determined that the reset was firmware initiated, so 8). the saved formatted configuration data was copied from the memory module EEPROM to the first memory controller using stackless instructions, and 9). a stack and variables were then initialized so that stack-based full memory initialization code was executed for the remaining memory controllers and their associated memory.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 8/14/2007

David L. Collins

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## **ENHANCED DYNAMIC MEMORY SIZING ALGORITHM**

